WHAT IS CLAIMED IS:

1. A semiconductor device having a copper (Cu) or Cu allow interconnect comprising:

an opening formed in a dielectric layer;

a composite barrier layer, comprising a layer of α-tantalum (α-Ta) over a tantalum nitride (TaN) layer, lining the opening; and

Cu or Cu alloy filling the opening and forming an interface with the composite barrier layer, wherein the composite barrier layer has an average surface roughness (Ra) at the interface with the Cu or Cu alloy of about 25Å to about 50Å.

2. The semiconductor device according to claim 1, wherein:

the opening is a dual damascene opening; and

the interconnect structure comprises a lower Cu or Cu alloy via connected to an upper Cu or Cu alloy line.

3. The semiconductor device according to claim 2, wherein the dielectric material has a dielectric constant less than about 3.9.

4. The semiconductor device according to claim 1, further comprising a graded tantalum nitride layer between the TaN layer lining the opening and the α-Ta layer.

5. The semiconductor device according to claim 4, wherein the graded tantalum nitride layer contains α-Ta ranging from about zero proximate the TaN layer to about 100% proximate the α-Ta layer.

6. The semiconductor device according to claim 4, wherein:

the TaN layer contains about 30 to 65 at.% nitrogen (N_2); and

the N_2 concentration of the graded tantalum nitride layer ranges from a value of about 30 to about 65 at.% proximate the TaN layer decreasing to about zero proximate the α-Ta layer.

7. The semiconductor device according to claims 4, wherein the ratio of the thickness of the combined α-Ta and graded tantalum nitride layers to the thickness of the TaN layer is about 200-400Å to about 20-100Å.

8. The semiconductor device according to claim 4, wherein the TaN, graded tantalum nitride and α-Ta layers have a combined thickness of about 50Å to about 500Å

9. The semiconductor device according to claim 4, wherein the opening is a dual damascene opening and the interconnect structure comprises a lower Cu or Cu alloy via in electrical contact with a lower metal feature and connected to an upper Cu or Cu alloy line.

10. The semiconductor device according to claim 9, wherein the interlayer dielectric comprises a dielectric material having a dielectric material having a dielectric constant less than about 3.9.

11. A method of manufacturing a semiconductor device, the method comprising:

forming an opening in a dielectric layer over a semiconductor wafer;

forming a composite barrier layer with an exposed surface having an average surface roughness (Ra) of about 25Å to about 50Å lining the opening, the composite barrier layer comprising a layer of α-tantalum (α-Ta) over an initial layer of tantalum nitride (TaN); and

filling the opening with copper (Cu) or a Cu alloy.

12. The method according to claim 11, further comprising:

depositing a graded tantalum nitride layer on the initial TaN layer lining the opening; and

depositing the α-Ta layer on the graded tantalum nitride layer.

13. The method according to claim 12, comprising:

depositing the TaN layer by ionized sputter deposition using a Ta target and a sufficiently high nitrogen (N_2) flow rate to poison the Ta target with N_2;

discontinuing the flow of N_2; and

depositing the graded tantalum nitride and α-Ta layers using the Ta target.

14. The method according to claim 12, comprising:

depositing the TaN layer using a nitrogen (N_2) flow rate; and

controlling the surface roughness (Ra) by varying:

a) the ratio of the thickness of the combined α-Ta and graded tantalum nitride layers to the thickness of the initial TaN layer; and/or

b) the N_2 flow rate during deposition of the TaN layer.

15. The method according to claim 14, comprising:
varying the ratio between about 50 to about 250.

16. The method according to claim 14, comprising varying the N_2 flow rate between about 10 to about 100 sccm.

17. The method according to claim 12, wherein the opening is formed in dielectric material having dielectric constant less than about 3.9.

18. The method according to claim 17, wherein the opening is a dual damascene opening, the method comprising filling the dual damascene opening to form a lower Cu or Cu alloy via in electrical contact with a lower metal feature and connected to an upper Cu or Cu alloy line.